REMARKS

Claims 1-28 remain pending in this application for which applicants seek reconsideration. Claims 15-28 have been withdrawn as directed to a non-elected invention.

Amendment

drawings change must be in red ink. Is it for the original drawings?

Applicants propose amending Figs. 1 and 3-24(b) to remove the informalities noted by the examiner and improve their form by removing all reference descriptions. The specification has been amended to remove those informalities identified by the examiner. Claims 1, 2, 4, 5, 13, and 15 have been amended to clarify the fifth region as an --offset-- region, as referred to in the present specification. See pages 20 (line 2) and 37 (line 5) for example. No new matter has been introduced.

Disclosure Objection

In drawing correction

All of the minor informalities identified by the examiner have been removed. Specifically, Fig. 24 has been clarified as a single figure. As to reference [159(a)] not being illustrated in Fig. 13, applicants submit that this reference appears in Fig. 13, next to element 159(b). As to reference 153c not being illustrated in Fig. 14, this reference has been corrected as 159c. The region 164 is now correctly recited as an n-type well. The sub-region having a surface boron concentration of about 5×10^{16} cm^{-3} has been clarified as region 169. The spelling of "more" has been corrected.

Art Rejection

The examiner rejected claims 1-12 under 35 U.S.C.§ 102(b) as anticipated by Kitamura (USP 5,705,842), and rejected claims 13 and 14 under 35 U.S.C. § 103(a) as unpatentable over Kitamura. Applicants traverse these rejections because Kitamura would not have taught the claimed offset region.

Independent claims 1 and 4 each call for an offset region comprised of a plurality of sub-regions aligned between the second region and the third region. As claimed, the impurity concentrations of the sub-regions are different from each other. When the device is OFF, the

offset region becomes a depletion layer, which is useful for raising the breakdown voltage. The examiner contends that Kitamura's regions 3, 31, and 4 correspond to the claimed fifth or offset region. Applicants disagree because Kitamura does not have an offset or fifth region that is defined by a plurality of subregions having different impurity concentrations. Kitamura's regions 3 and 31 are not offset regions because they do not become a depletion layer when the device is OFF. As Kitamura only has an offset region 4 with no subregions having different impurity concentrations, Kitamura would not have anticipated or taught the claimed invention.

Conclusion

Applicants submit that claims 1-14 patentably distinguish over the applied reference and thus urge the examiner to issue an early Notice of Allowance. Should the examiner have any issues concerning this reply or any other outstanding issues remaining in this application, applicants urge the examiner to contact the undersigned to expedite prosecution.

Respectfully submitted,

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ATTACHMENT

MARKED UP VERSION

IN THE SPECIFICATION:

Page 17, the paragraph appearing in lines 1-3 has been amended as follows:

--Fig. 14 shows the simulated distribution of the electric field strength [(a)] across the cross-section [(b)] of the semiconductor device according to the third embodiment of the invention.--

Pages 26-27, the paragraph spanning these pages has been amended as follows:

--It has been confirmed by simulation that the electric field strength distributes across the semiconductor structure described above, as illustrated in Fig. 14[(a)]. The electric field strengths EC, ED, EE and EF at the points C, D, E and F are lower than 2×10^5 V/cm. The electric field strength is low at these points due to (1) the depletion layer expanding from the pn-junction between p-type base region 153 and n-type well region 152 to n-type well region 152 and (2) the depletion layer expanding from the pn-junction between n-type well region 152 and p-type diffusion region 159 to the portion of p-type diffusion region 159 near n-type drain region 154. The breakdown voltage of the device is determined by the breakdown voltage of the junction portion (point G) between n-type well region 152 and p-type substrate 151 below n-type drain region 154.--

Page 27, the first full paragraph has been amended as follows:

--The structure described above facilitates securing a stable breakdown voltage at high temperature and under the application of high voltage over a long period of time. The volume of n-type well region 152 below p-type diffusion sub-region [153c] 159c, which causes the most part of the on-resistance, is increased in the structure of the invention over that exhibited in the conventional semiconductor structure, and the on-resistance is reduced. When n-type well region 152 is formed by diffusion, the heavily doped region is expanded, and the on-resistance is reduced by 5%, as compared to that of the conventional semiconductor structure.--

Pages 27-28, the paragraph spanning these pages has been amended as follows:

--Fig. 15 is a cross-sectional view of a semiconductor device exhibiting a high breakdown voltage according to a fourth embodiment of the invention. Referring to Fig. 15, the semiconductor device according to the fourth embodiment includes a p-type substrate 151 with high resistivity of 150 ohm-cm, an n-type well region 164 in the surface portion of p-type substrate 151, and a p-type base region 153 in the surface portion of n-type well region 164. The [p-type] n-type well region 164 includes a first n-type well sub-region 165, a second n-type well sub-region 166, and a third n-type well sub-region 167, with the impurity concentrations for each sub-region differing from each other. The surface concentration is 2.4×10^{16} cm^{-3} for first well sub-region 165, 3.0×10^{16} cm^{-3} for second well sub-region 166, and 3.6×10^{16} cm^{-3} for third well sub-region 167. The diffusion depth is 4 micrometers for first well sub-region 165, 5 micrometers for second well sub-region 166, and 6 micrometers for third well sub-region 167. For example, the width Lp_1 is about 25 micrometers, the width Lp_2 is about 20 micrometers, and the width Lp_3 is about 25 micrometers. A p-type diffusion region 169 (p-type offset region) including three diffusion sub-regions, in which the surface concentrations and the diffusion depths differ from each other, is formed in the surface portion of a section Ld of n-type well region 164 (an n-type drift region). The width of the section Ld is about 70 micrometers to guarantee the breakdown voltage of 700 V. To form p-type diffusion region 169, boron ions are doped collectively to the diffusion depth of 1.0 micrometer at the surface concentration of 5×10^{16} cm^{-3}. The boron diffusion depth 168 is shown by a broken line. As a result, a first diffusion sub-region 169a (p-type) is in the surface portion of first well sub-region 165, a second diffusion sub-region 169b (p-type) is in the surface portion of second well sub-region 166, and a third diffusion sub-region 169c (p-type) is in the surface portion of third well sub-region 167.--

Pages 28-29, the paragraph spanning these pages has been amended as follows:

--In the actual manufacturing process, phosphorus ions are implanted to the portion of the n-type well region that includes the sections Lp_1, Lp_2 and Lp_3. The dose

amount is that amount that will produce, after heat treatment, a surface phosphorus concentration of about 2.4×10^{16} cm^{-3}. The implanted phosphorus ions are thermally driven at 1150°C for 10 hours. Phosphorus ions are added to the sections Lp_2 and Lp_3 at the dose amount that will produce, after heat treatment, a surface phosphorus concentration in the sections Lp_2 and Lp_3 of about 3.0×10^{16} cm^{-3}. And phosphorus ions are added to the section Lp_3 at a dose amount that, after heat treatment, will produce a surface phosphorus concentration in section Lp_3 of about 3.6×10^{16} cm^{-3}. Then, to form p-type diffusion region 169, boron ions are doped into the region that includes the sections Lp_1, Lp_2 and Lp_3 at a dose amount that, after heat treatment, will produce a surface boron concentration of the region 169 of about 5×10^{16} cm^{-3}. The doped boron ions are driven thermally.--

Page 35, the first full paragraph has been amended as follows:

--Referring now to Fig. 17(d), a p-type base region and a part of the p-type offset region are formed by boron ion implantation 13 using a patterned photoresist 11 as a mask. The dose amount of boron ions 12 is set more than around the boron dose amount used in the foregoing region A.--

IN THE CLAIMS:

Claims 1, 2, 4, 5, 13, and 15 have been amended as follows:

--1. (Amended) A semiconductor device exhibiting a high breakdown voltage, the semiconductor device comprising:

a first region of a first conductivity type;

a second region of a second conductivity type formed selectively in the surface portion of the first region;

a third region of the first conductivity type formed selectively in the surface portion of the first region, the second region and the third region being spaced apart from each other;

a fourth region of the first conductivity type formed selectively in the surface portion of the second region;

[a fifth] an offset region of the second conductivity type formed selectively in the surface portion of the first region between the second region and the third region;

a first insulation film on the [fifth] offset region;

a gate electrode above the extended portion of the second region extending between the fourth region and the first region with a gate insulation film interposed between the extended portion of the second region and the gate electrode;

a first main electrode on the fourth region; and

a second main electrode on the third region;

wherein the [fifth] offset region comprises a plurality of sub-regions aligned between the second region and the third region, the impurity concentrations of the sub-regions being different from each other.

2. (Amended) The semiconductor device according to Claim 1, wherein the depths of the sub-regions of the [fifth] second region are different from each other.--

--4. (Amended) A semiconductor device exhibiting a high breakdown voltage, the semiconductor device comprising:

a semiconductor substrate of a second conductivity type;

a first region of a first conductivity type formed selectively in the surface portion of the semiconductor substrate;

a second region of the second conductivity type formed selectively in the surface portion of the semiconductor substrate;

a third region of the first conductivity type formed selectively in the surface portion of the first region;

the second region and the third region being spaced apart from each other;

a fourth region of the first conductivity type formed selectively in the surface portion of the second region;

[a fifth] an offset region of the second conductivity type formed selectively in the surface portion of the first region between the second region and the third region;

a first insulation film on the [fifth] offset region;

a gate electrode above the extended portion of the second region extending between the fourth region and the first region with a gate insulation film interposed between the extended portion of the second region and the gate electrode;

a first main electrode on the fourth region; and

a second main electrode on the third region;

wherein the [fifth] offset region comprises a plurality of sub-regions aligned between the second region and the third region, the impurity concentrations of the sub-regions being different from each other.

5. (Amended) The semiconductor device according to Claim 4, wherein the depths of the sub-regions of the [fifth] offset region are different from each other.--

--13. (Amended) The semiconductor device according to Claim 1, wherein the surface impurity concentration of the [fifth] offset region of the second conductivity type is changed by adding an impurity of the first conductivity type, the amount thereof being less than the amount of the impurity of the second conductivity type in the [fifth] offset region.

14. (Amended) The semiconductor device according to Claim 4, wherein the surface impurity concentration of the [fifth] offset region of the second conductivity type is changed by adding an impurity of the first conductivity type, the amount thereof being less than the amount of the impurity of the second conductivity type in the [fifth] offset region.--